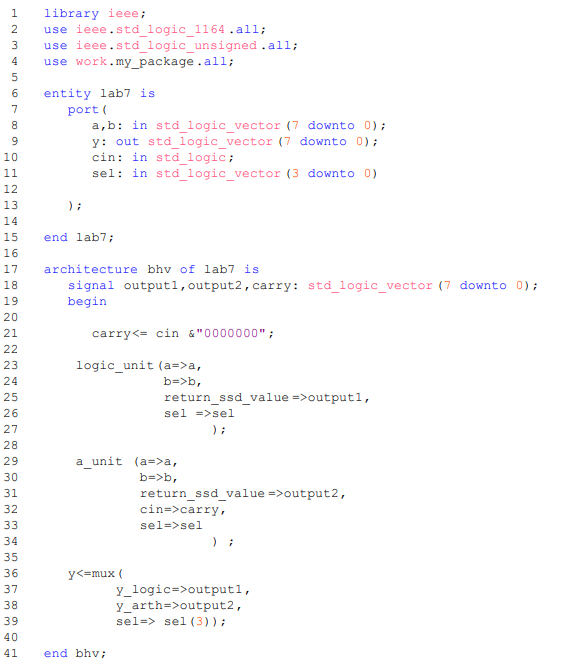
**INTRODUCTION:**

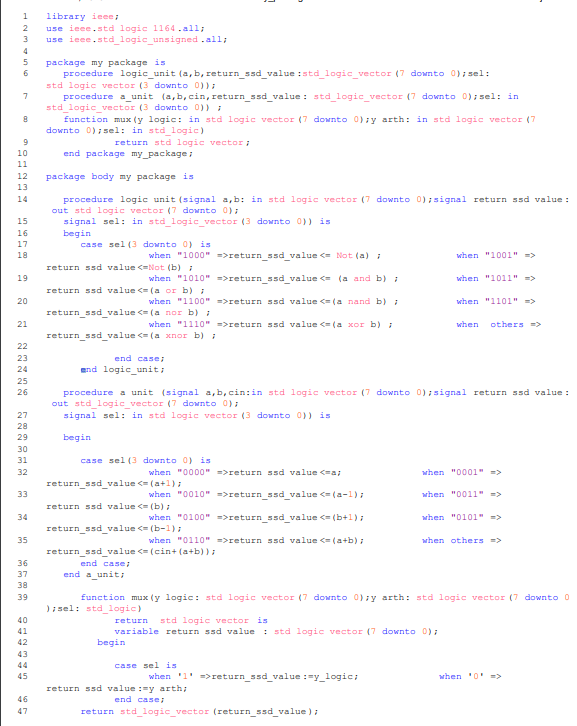
**A package in VHDL is a collection of functions, procedures, shared variables, constants, attributes, and components.** A package file is often (but not always) used in conjunction with a unique VHDL library. Packages are most often used to group together all of the code specific to a Library. Packages can have two parts: a **declaration** and a **body**, though the body is not necessarily required. The declarations section contains the prototypes for the functions and procedures that are defined. The body section contains the actual implementation of the functions and procedures. If you've used C before, the declaration section is similar to a .h file.

**LAB TASKS:**

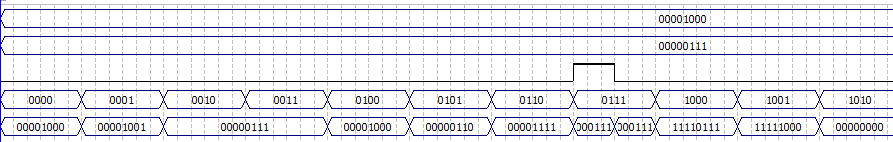
**Task 1:**

1. VHDL Code





1. Results (VWF)



# CONCLUSION:

In this lab I learned how to use functions and procedures.